



MG127 BLE Transceiver  
Data Sheet

Revision History:

| Rev. No. | History                          | Issue Date    | Remark      |
|----------|----------------------------------|---------------|-------------|
| 0.1      | Initial issue                    | April 3, 2015 | Preliminary |
| 0.2      | update pinout info               | Oct 23, 2015  | Preliminary |
| 0.3      | Add Electrical Characteristic    | Dec 3, 2015   | Preliminary |
| 0.4      | Update SPI timing chart          | Jan 18, 2016  | Preliminary |
| 0.5      | Update Electrical Characteristic | Sep 19, 2016  | Preliminary |

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## 1. Overview

MG BLE chip is a single mode BLE RF transceiver with software configurable registers, embedded packet handling engine, and designed for ultra low power Bluetooth Smart Devices.

The chips are configured and operated via the 3-wire SPI(Serial Peripheral Interface).

Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range(1.9~3.6V).

### 1.1 Features

- Radio

Worldwide 2.4GHz ISM band operation with 2MHz channel spacing

Common RX and TX pins

GFSK modulation

1Mbps air data rate

- Transmitter

Programmable output power: -50~4 dBm, without an external RF PA

20mA at 0dBm output power

- Receiver

Integrated channel filters

-85dBm sensitivity

Programmable LNA gain

- Baseband

Dedicated logic performs:

Cyclic redundancy check



Data whitening

Access code correlation

- Host Interface

3-wire SPI

Max 10Mbps

- Power Management

Integrated voltage regulator

1.9 to 3.6V supply range

Idle modes with fast start-up times for advanced power management

3uA in sleep mode

- Low cost BOM

Provides a single-ended RF TX / RX port pin

No matching components needed

Built-in 32.768KHz oscillator, no need external RTC crystal

Support low cost crystal(16MHz)

## 1.2 Typical Application

- Beacon
- Remote Controller



### 1.3 Block Diagram

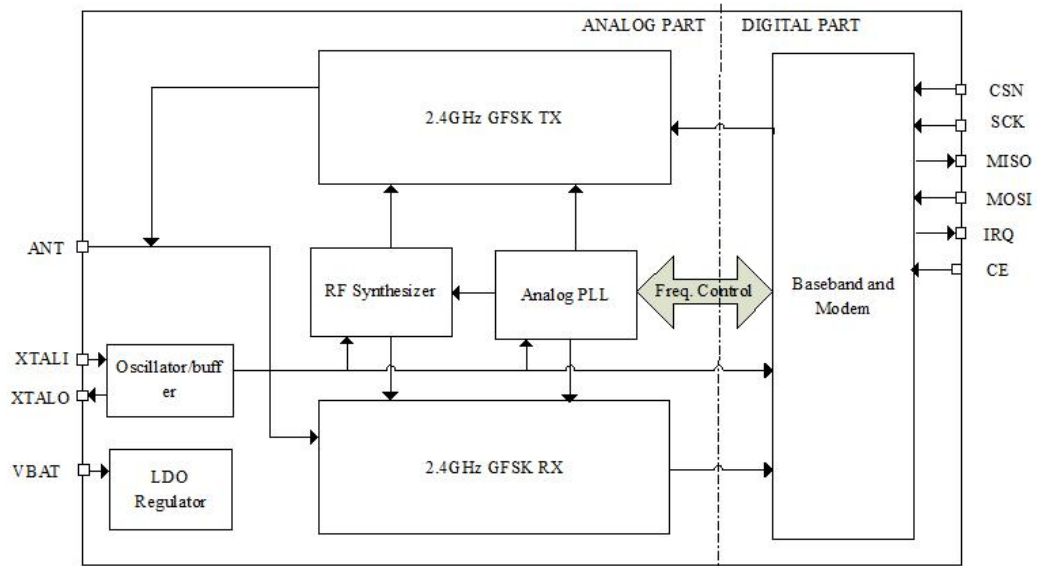


Figure1.1 Block Diagram

### 2. Pin Description

| Pin No. | Symbol | I/O   | Function Description        |
|---------|--------|-------|-----------------------------|
| 1       | SCK    | DI    | SPI Clock                   |
| 2       | DVDD   | Power | Digital VDD 1.2v Output     |
| 3       | MOSI   | DI    | SPI Slave Data Input/Output |
| 4       | XTALO  | AO    | Crystal Pin                 |
| 5       | XTALI  | AI    | Crystal Pin                 |
| 6       | ANT    | RF    | Antenna interface           |
| 7       | VBAT   | Power | Power Supply                |
| 8       | IRQ    | DO    | Maskable interrupt pin      |
| 9       | CT     | DI    | Test use                    |
| 10      | CSN    | DI    | SPI Chip Select             |
| 11      | GND    | Power | *Down bonding to Ground(0V) |

Table2.1 MG127 Pin Description



### 3. Example Application Schematic

MG127 with single ended RF output, crystal and decoupling capacitors.

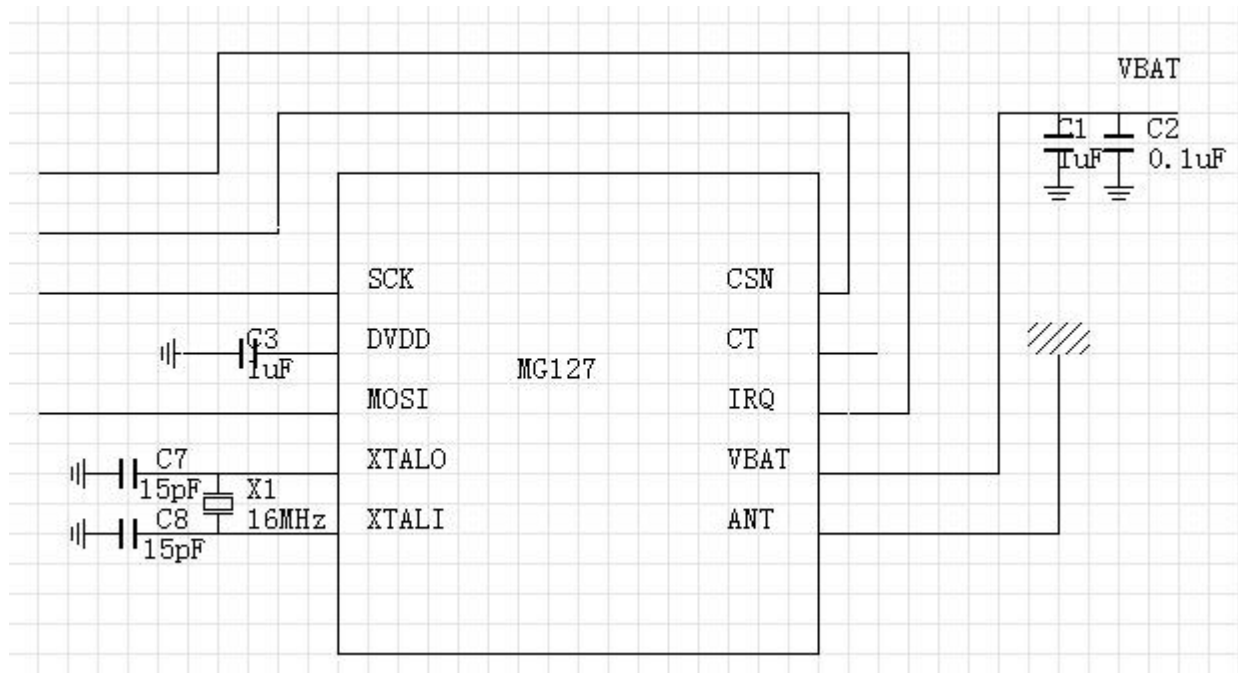


Figure 3.1 Example Application Schematic

### 4. Data and Control Interface

The data and control interface gives you access to all the features in the chip. The data and control interface consists of the following 4 digital signals:

- IRQ (this signal is active low and is controlled by maskable interrupt sources)
- CSN (SPI signal)
- SCK (SPI signal)
- MOSI (SPI signal)

#### 4.1 Features

- 3-wire SPI serial interface, as slave
- Easily configurable register map



## 4.2 SPI Timing

The interface supports SPI. SPI operation and timing is given in Figure 4.2.1. The device must be in one of the standby modes or sleep mode before writing to the configuration registers.

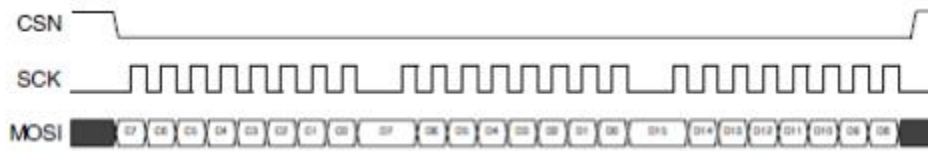


Figure 4.2.1 SPI read operation

## 4.3 Interrupt

The chip has an active low interrupt (IRQ) pin. The IRQ pin is activated by the state machine, and is resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the register is used to select the IRQ sources that are allowed to assert the IRQ pin. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

## 5 Register Map

You can configure and control the radio chip by accessing the register map through the SPI using read and write commands.

## 6. Electrical Characteristic

Conditions: VDD = +3V, VSS = 0V, TA = - 40°C to + 85°C

| Symbol                          | Parameter             | Notes | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------------|-------|------|------|------|------|
| Operating Conditions            |                       |       |      |      |      |      |
| VDD                             | Supply voltage        |       | 1.9  | 3.0  | 3.6  | V    |
| TEMP                            | Operating Temperature |       | -40  | +27  | +85  | °C   |
| General RF condition            |                       |       |      |      |      |      |
| f <sub>OP</sub>                 | Operating frequency   |       | 2402 |      | 2480 | MHz  |
| Transmitter Operation condition |                       |       |      |      |      |      |
| P <sub>RF</sub>                 | Maximum output power  |       |      |      | +4   | dBm  |

Table 6.1 Electrical Specification



## 7. Current Consumption

Table 7.1 shows total typical current consumption measured at the battery.

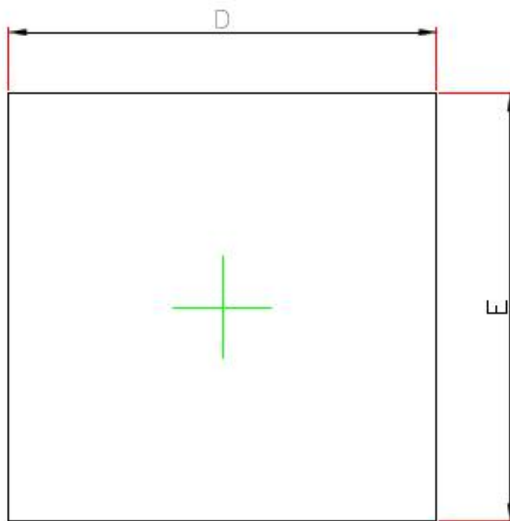
| Mode      | Description                       | Total Typical Current at 3.0v |
|-----------|-----------------------------------|-------------------------------|
| sleep     | Sleep. wakeup through SPI command | 3 $\mu$ A                     |
| TX active | In transmitting                   | 20 mA @ 0dBm output power     |

*Table 7.1 Current Consumption*

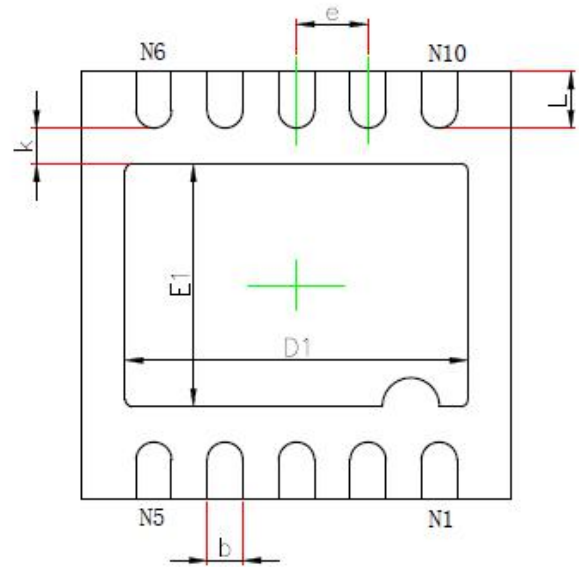




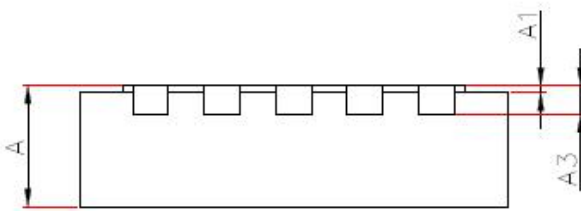
## 8. Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

| Symbol | Dimensions in Millimeters |       | Dimensions in Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min.                      | Max.  | Min.                 | Max.  |
| D/E    | 2.924                     | 3.076 | 0.115                | 0.121 |
| D1     | 2.300                     | 2.500 | 0.091                | 0.098 |
| E1     | 1.600                     | 1.800 | 0.063                | 0.071 |
| k      | 0.200 MIN.                |       | 0.008 MIN.           |       |
| b      | 0.200                     | 0.300 | 0.008                | 0.012 |
| e      | 0.500 TYP.                |       | 0.020 TYP.           |       |
| L      | 0.324                     | 0.476 | 0.013                | 0.019 |

Table 8.1 DFN3x3-10 Package outline